January 27, 2000

Informations and analysis concerning the yield problems encountered on the HAMAC chip.

E. DELAGNES. CEA/DAPNIA/SEI

Ref ED2.1.1999

1. Introduction.

The yield obtained for the HAMAC circuits extracted from different wafers from different batches is very variable. The table 1 summarizes the list of the batches tested and the results extracted.

BATCH/WAFER INTERNAL IDENTIFICATION	V1.1	V1.2	V2 wafer12	V2 wafer4	V2 wafer4 mirrored	V3
BATH NUMBER	Z25291A	?	Z28451	Z28451	Z28451	230355
WAFER NUMBER	?	?	W12	W4	W4	?
DELIVERY DATE	June 98	Aug 98	June 99	Aug 99	Aug 99	DEC 99
BACKSIDE METALLIZED	NO	NO	NO	YES	YES	NO
NUMBER OF TESTED CHIPS	30	30	20	48	49	18
NUMBER OF GOOD CHIP	27	24	10	39	43	2
CHIP WITH 1or 2 bad cell	2	4	8	6	4	14
Other Problem	1	2	2	3	2	2
'Yield'	90%	80%	50%	81%	87%	11%

Table 1 : list of the chip tested. ↳ high defect density expected

A good chip is defined as a chip within the specification (not only functional yield)

This table shows that the larger part of the failures concerns only one or two storage cell in the chip.

2. Short description of the HAMAC circuit.

The HAMAC circuit is a 16 channels * 144 cells analog memory. Its function is to sample and memorize, during duration up to tens microsecond, an analog information with a precision better than 0.5 mV. One acceptance criteria for the chip is that the pedestal

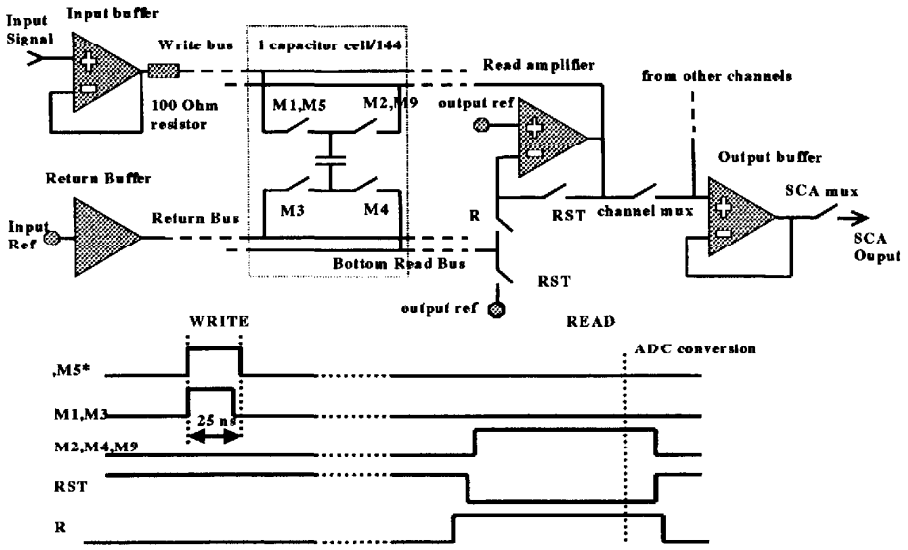


Fig 1 : schematic of one channel.

value of one cell should not spread from the mean value obtained for the 143 other cells of the same channel of more than 2mV.

The write and read amplifiers and additional circuitry are common to the 144 capacitors of a same channel (see fig2). The write and read commands are common to the 16 capacitors of a same column. So that, a failure observed on a single storage cell can be explained only at the storage cell level.

The 16 channels of a chip are divided into 4 groups of four including 3 signal channels and 1 reference channel. The input of a reference channel is grounded . Its output is externally subtracted to the one of the 3 other channels of the same group during the read-out operation , allowing thus common mode noise rejection.

Thus a problem on a cell of a reference channel will affect the same cell on the 3 signal channels of the same group.

The layout and the schematic of an elementary storage cell is shown in fig2 .

The NMOS and PMOS transistors are grouped 2 by 2 in same wells.
Vss is –1.7V
Vdd is +3.3v
wb is the write bus with signals in the range of –0.9V to 2.5V
wrb is the write return bus set at 0V
rb is the read bus (-0.9Vto 2.5V) (rb =0V duration phases other than the read operation)
rrb is the read return bus (0V high impedance point)
All the switches commands are between vss and vdd levels.

During the write operation, M1,M3,M5 switches are closed while the other switches are open. The sampling and memorization is performed by sequentially opening the M3+M1, then the M5 switches. All the switches are closed, awaiting the read operation. At this time M2,M4

and M9 switches are closed, putting the storage capacitor in feedback across the read amplifier.

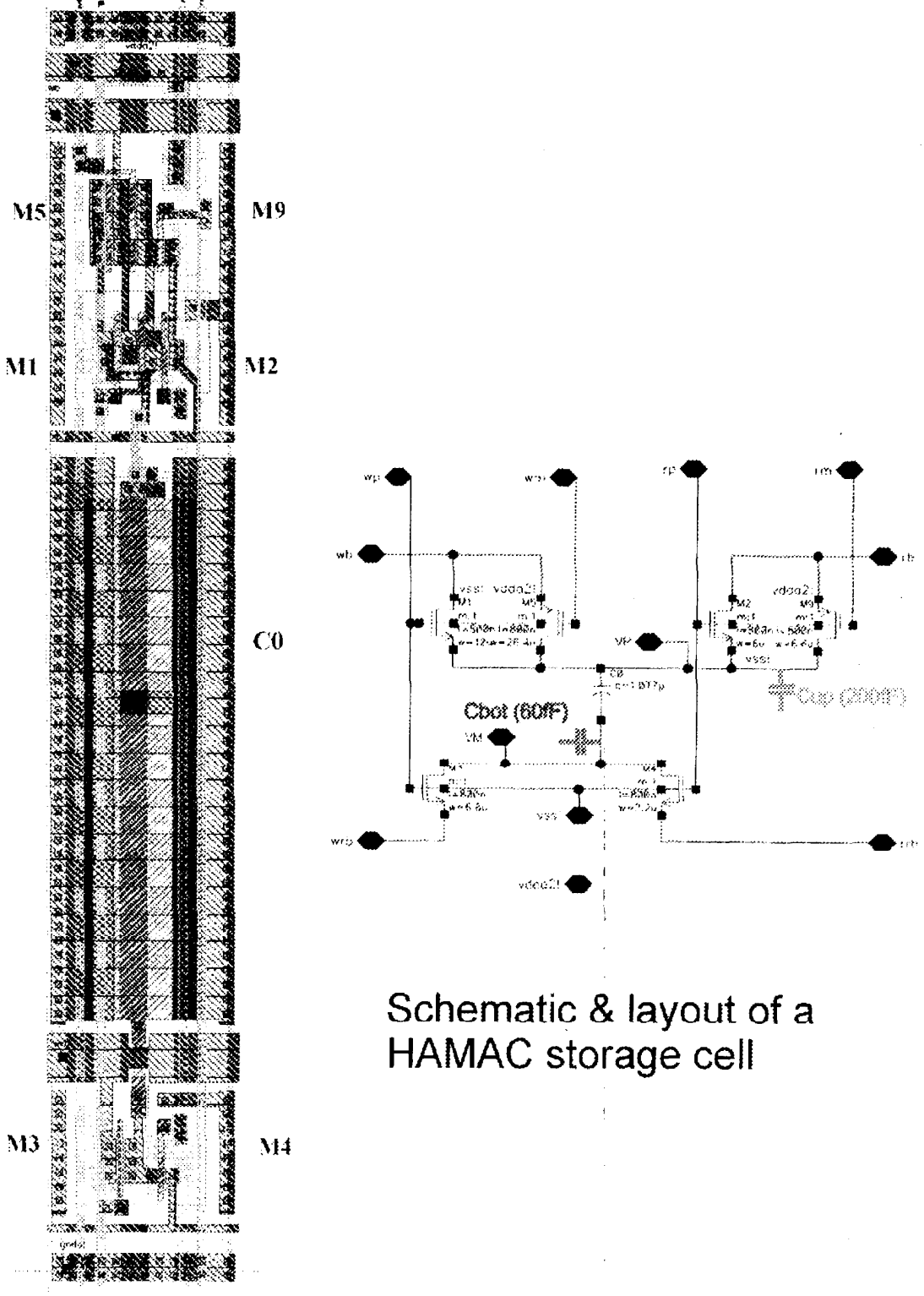


fig 2 : layout and schematic of a storage cell.

3. Problems observed on V2 wafer 12 chips.

Around 50% of the chips presented the following failure:

The DC level obtained on one or two single cells in the chip was different from the mean one by one to few hundred mV. When performing a DC linearity on this particular cells, it appeared that these cells was not completely dead, but presented a very unusual behavior : different gain and high non-linearity. The magnitude of this effect was unaffected by the duration between the write and read operations.

This problem was correlated by Thierry Corbiere to a 'high density of defects' on this particular wafer.

Defects of the same type are also present, but less usual, on all the other wafers (including V3 one).

4. Problems observed on V3 chips.

a) description.

Few chips have cells presenting the same problem than the one described in 3.
But a large majority of the chips presents the following failure :

- When the time between write and read (trw) is smaller than 2 us, one or two cells of the chip present a DC value different from the mean one by 2mV up to few hundred mV (depending on the chip). This value can be higher or smaller than the mean one . But for these particular cells, the DC linearity is not abnormal, and the gain of the cell is exactly the same than the one of its neighbors. In this test conditions, 5 chips are considered as good.

- When the time between write and read is increased up to 500us, the shift observed on the bad cells is multiplied by at least 100. Moreover, the same type of failures, but with lower level, are observed on new cells (typically 20 in a chip, 1% of the cells in a chip). The bad cells have again a linear behavior . In these conditions, the number of good chip is then reduced to 2 !!.

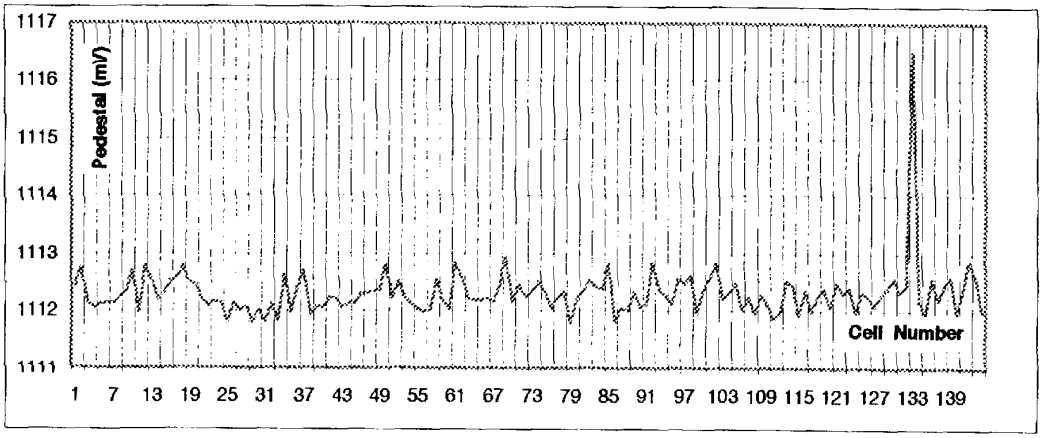


Fig 3 : Baseline of one channel in the case of a short duration between write and read. The cell 135 is obviously bad.

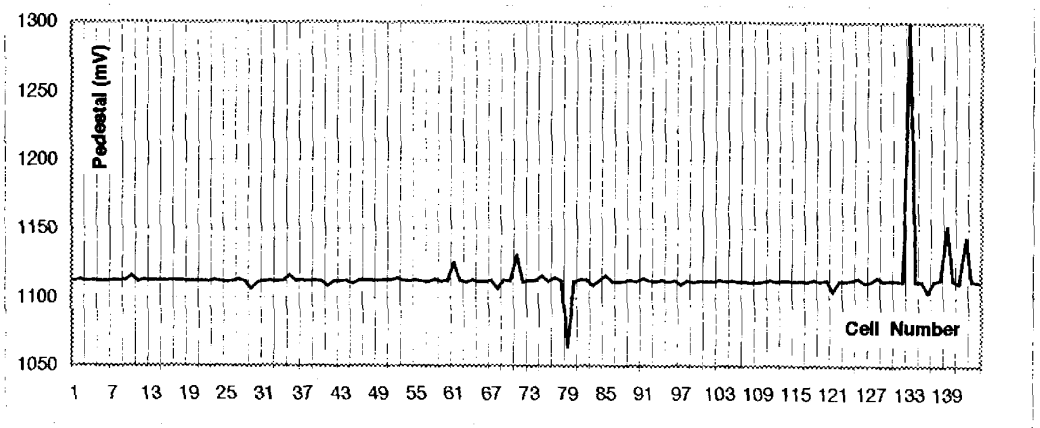


Fig 4 : Baseline of one channel in the case of a 500us duration between write and read. The cell 135 is worst and other bad cells appear.

To summarize, the bad cells present an abnormal pedestal which is depending on the duration between the write and read operations.
The timing dependency of this failure tends to be an evidence of a leakage somewhere in the cell (switches or capacitor).

b) Sign of the pedestal Shift

After a deeper analysis, it has been shown that the bad cells showing negative pedestal shift (as cell 79 in fig 4) correspond to bad cells in a reference channel. Then, the shift, positive on a reference channel ,becomes negative when subtracted to a signal channel. We have checked that a negative shift is always common the 3 channels of a group.

All the pedestal shifts are positive.

c) Variation of the shift with time.

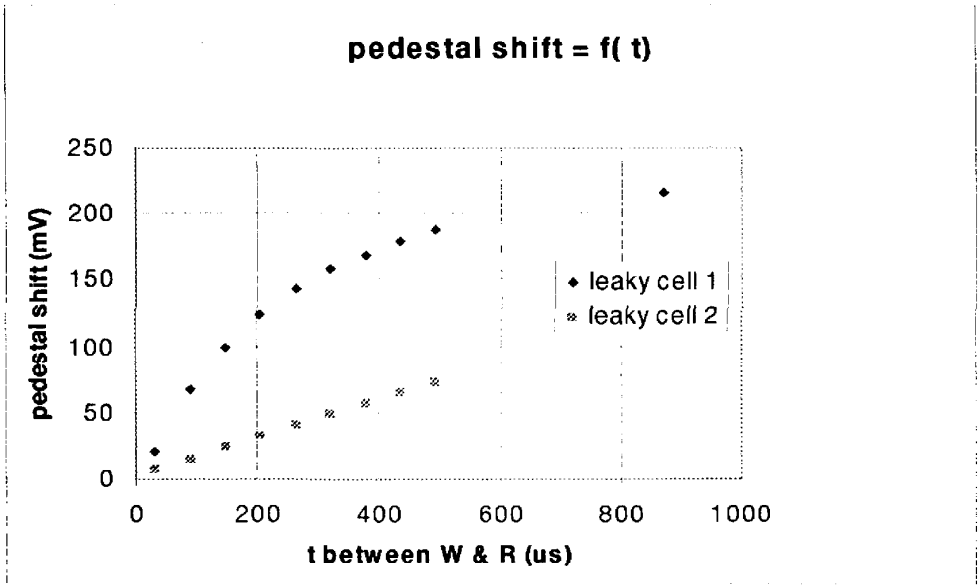


Fig 5 : pedestal shift with time on 2 cell.

Figure 5 shows the increase of the pedestal shift with the trw (time between write and read) for two cells. This variation seems to be exponential (different time constant for the two cells, tau=260us for the more leaky).
This behavior is characteristic of a resistive discharge (non with a constant current).

c) Variation of the voltage shift with the return bus voltage.

The return buffer is only a NMOS source-follower (see fig1). In the chip, a servo-control system has been implemented in order to set the return bus voltage to 0V, the gate of the NMOS source-follower is then 1.5V. By setting a voltage directly on the gate of the follower with a low impedance, we can 'break' the servo-control and then modify the voltage of the return bus.

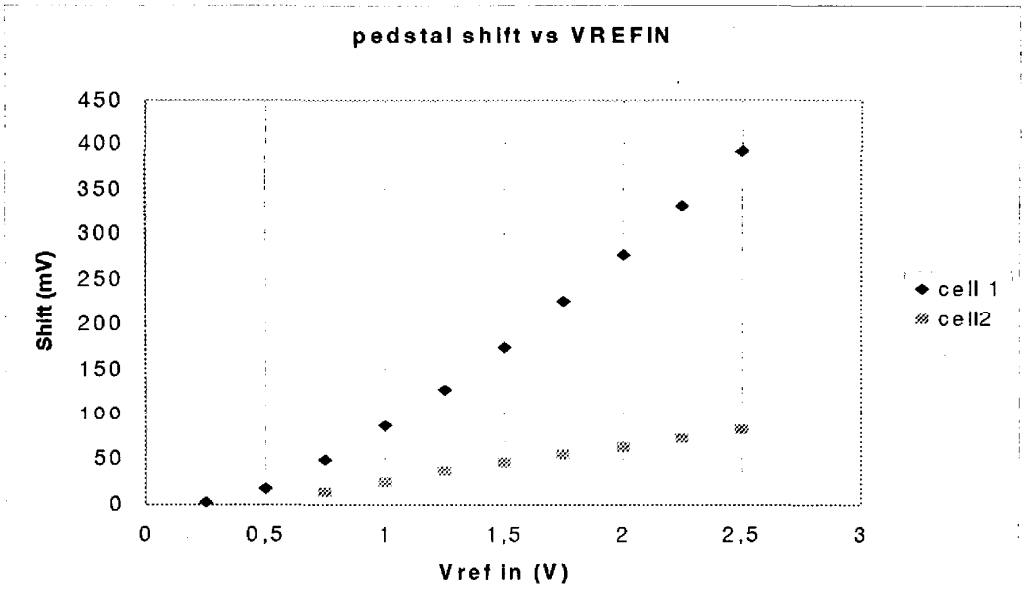


Fig 6 : Pedestal shift vs gate voltage of the NMOS follower.

Fig 6 shows the variation of the voltage shift of a leaky cell with the voltage applied on the gate of the return NMOS follower.

For Voltage > 1 V (corresponding to a return bus voltage > -0.2V) the variation is linear.

For voltage <0.25 (corresponding to a return bus voltage < -0.75V) the shift becomes negligible.

d) Variation of the voltage shift with the signal input voltage.

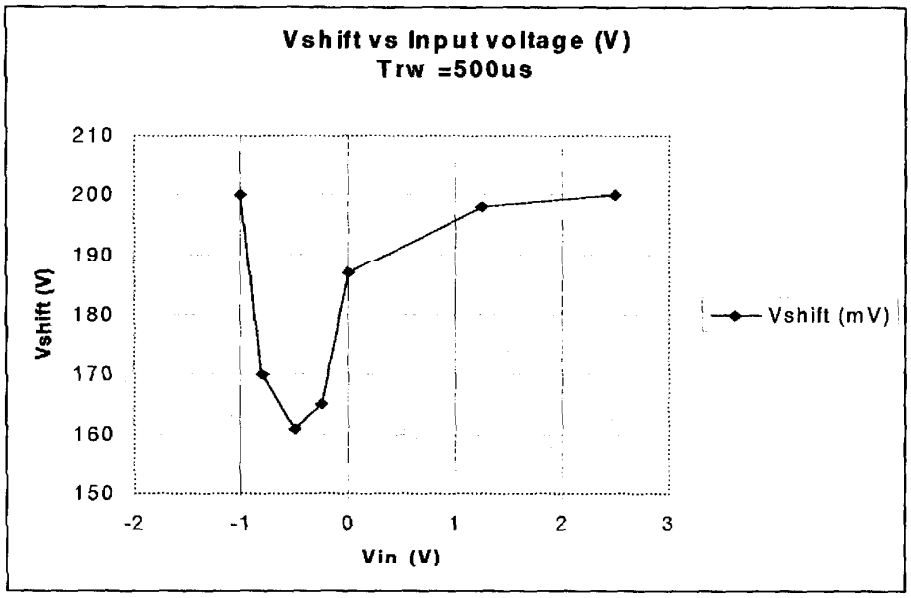


Fig 7 : Pedestal shift vs DC voltage of the input signal.

The variation of the shift of leaky cells with the DC level of the input signal is small. It explains why the linearity of bad cells are nearly unaffected.
The small variation of the shift with the input voltage excludes a restive leakage of the storage capacitance itself.

e) Simulations and analysis.

We have tried to simulate this leakage effect by inserting resistor in various places of the storage cell (VP to wb, VP to VDD, VM to VSS, VM to wrb...), (see fig2).
The behaviours described in a) to d) are fully or partially reproduced in simulation if we add a resistor (Rleak= 1-2 GOhm) between VM and VSS .

In these conditions :

As shown in figure 8, once the signal is sampled, Cdown and (Cup in serie with Cs) are discharged to VSS with a time constant Tleak= Rleak*(Cdown+(Cup.Cs/(Cup+Cs))).

The voltage shift obtained , after reading back can be calculated at first order as :

Vshift = (VM-Vss) . exp (- trw / Tleak) . (Cs/Cdown + Cup /(Cup+Cs)) (VM is the voltage of VM)
= (VM-Vss) / 4.6 . exp (- trw / Tleak)
=370mV . exp (-trw/ Tleak) (with the values extracted from layout)

in quite good accordance with b) and c) (sign and exponential variation), but the effect seems to be 1.5 time larger than the one measured (Cup and Cdown over estimated ? ?, or leakage to a voltage different from vss)

The different levels of leakage measured for different bad cells in a chip can be due to different Rleak values, and then to different time constants .

Fig 9 shows the simulated pedestal shift variation vs trw (time between read and write).

The fig 10 shows a simulated variation of Vshift vs Vin in good agreement with the measurements shown on fig 7 (same shape).

The fig 11 shows the simulated variation of the pedestal shift due to a resistive leakage versus the reference input voltage (input of NMOS follower) .
This curve is similar to the one measured (fig 6), but shifted by 1V.
The same curve, also plotted in fig11, but simulated with leakage network composed by a resistor in serie with 2 diodes. The simulated behavior is then nearer to the one measured (fig 6).

f) Possible causes of the leakage.

The measured behaviour of bad cells can be reproduced by adding a leakage resistor in serie with two diodes between the bottom plate of the storage cell (VM) and VSS.

This leakage network can be localized betwen any elements connected to VM or VSS :

The following nodes are connected together to VM :
Drain of M3, drain of M4.
Bottom plate of Cs (Poly plate).
Polysilicon connection between M3,M4 and Cs

In the same area, during the time between write and read operations, the voltage of the following nodes is VSS:
Gate of M3 and M4.
Body of M3 and M4.
Cs guard rings.
M1 shield over Cs.

DECHARGE de wbot et wtop R_{leak} 6 Ω . 01/24/2000 18:03:58

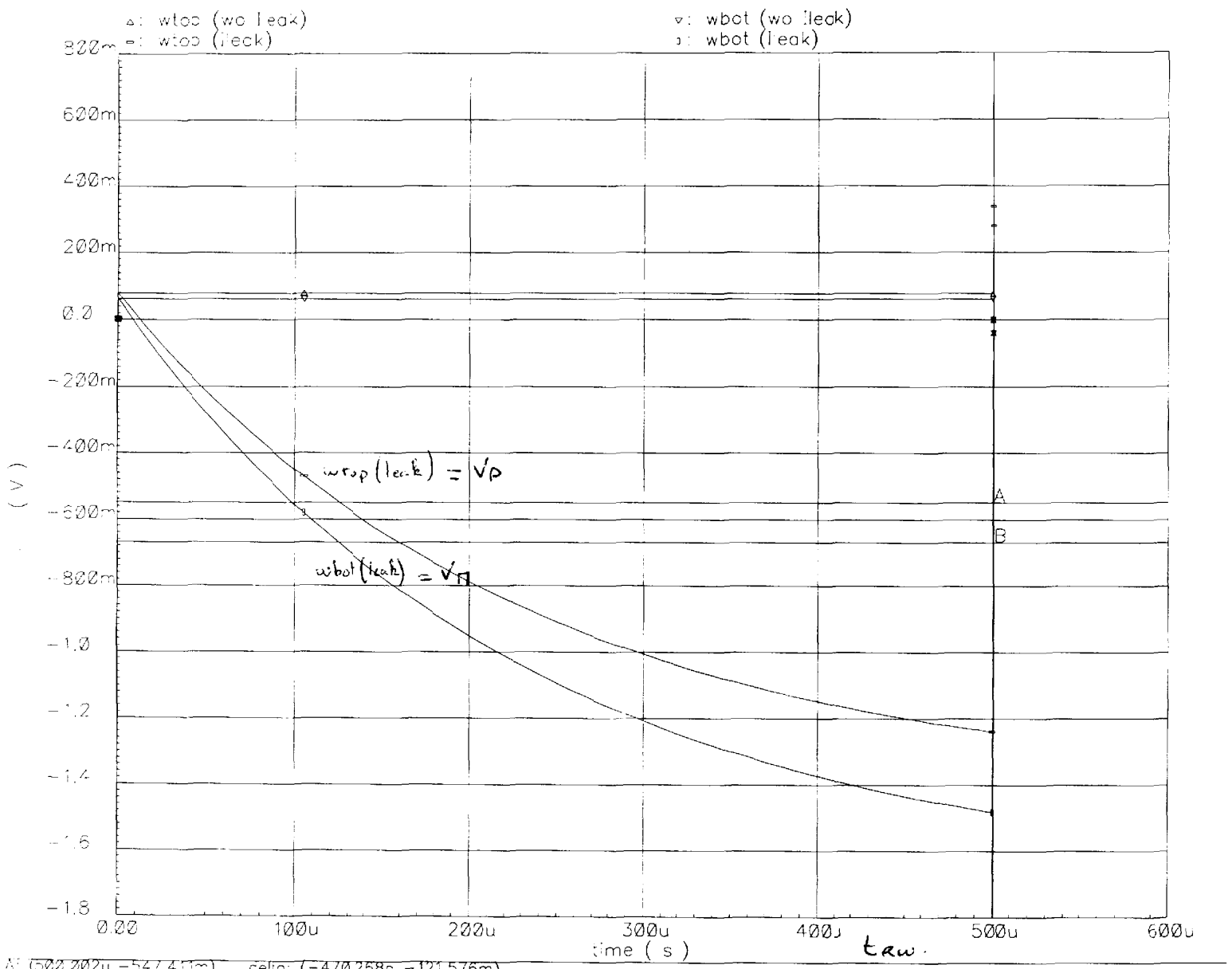


Fig 8 leakage $V_n - V_{ss} \Rightarrow$ offset on V_n and V_p.
$R = 6\,G\Omega$

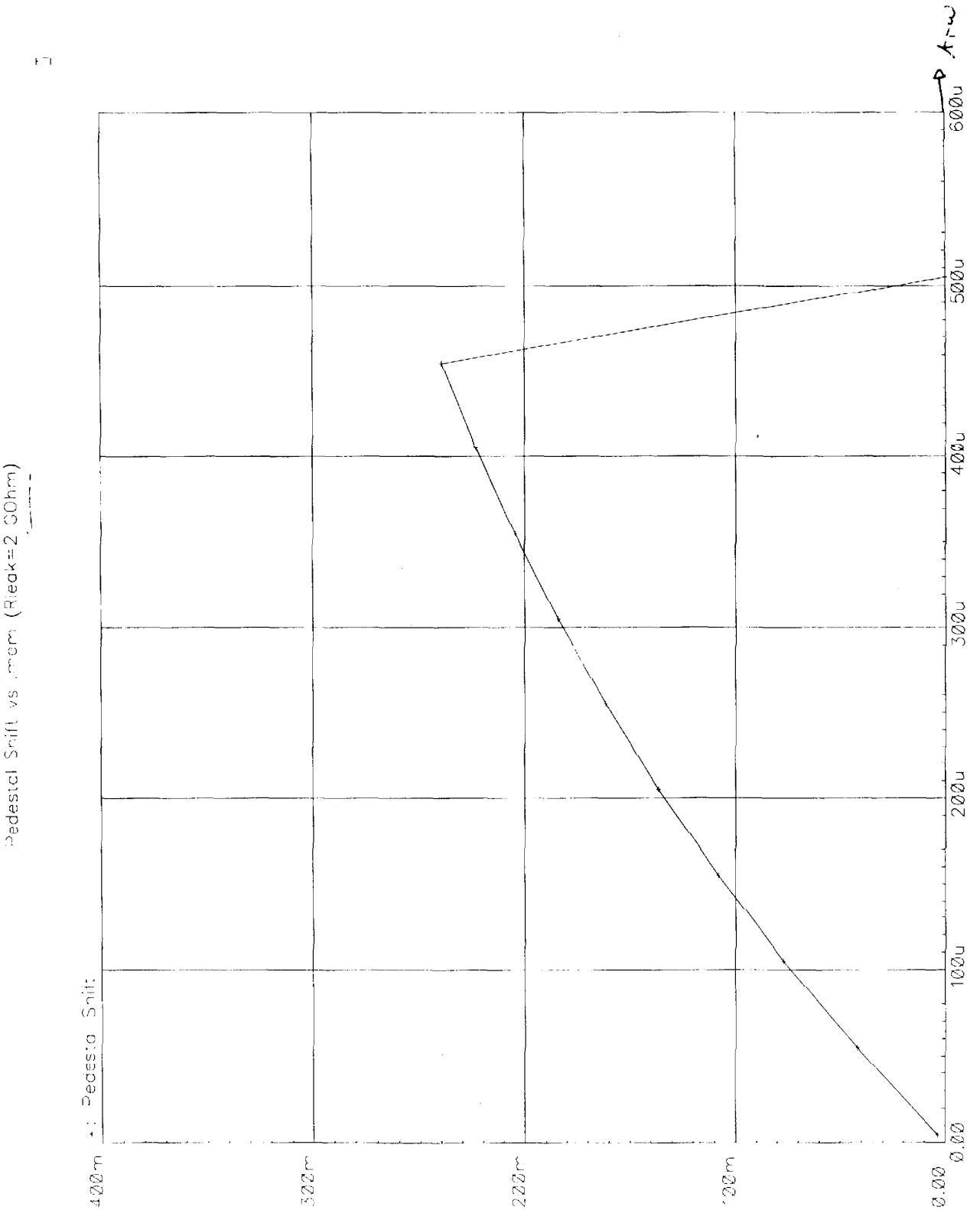
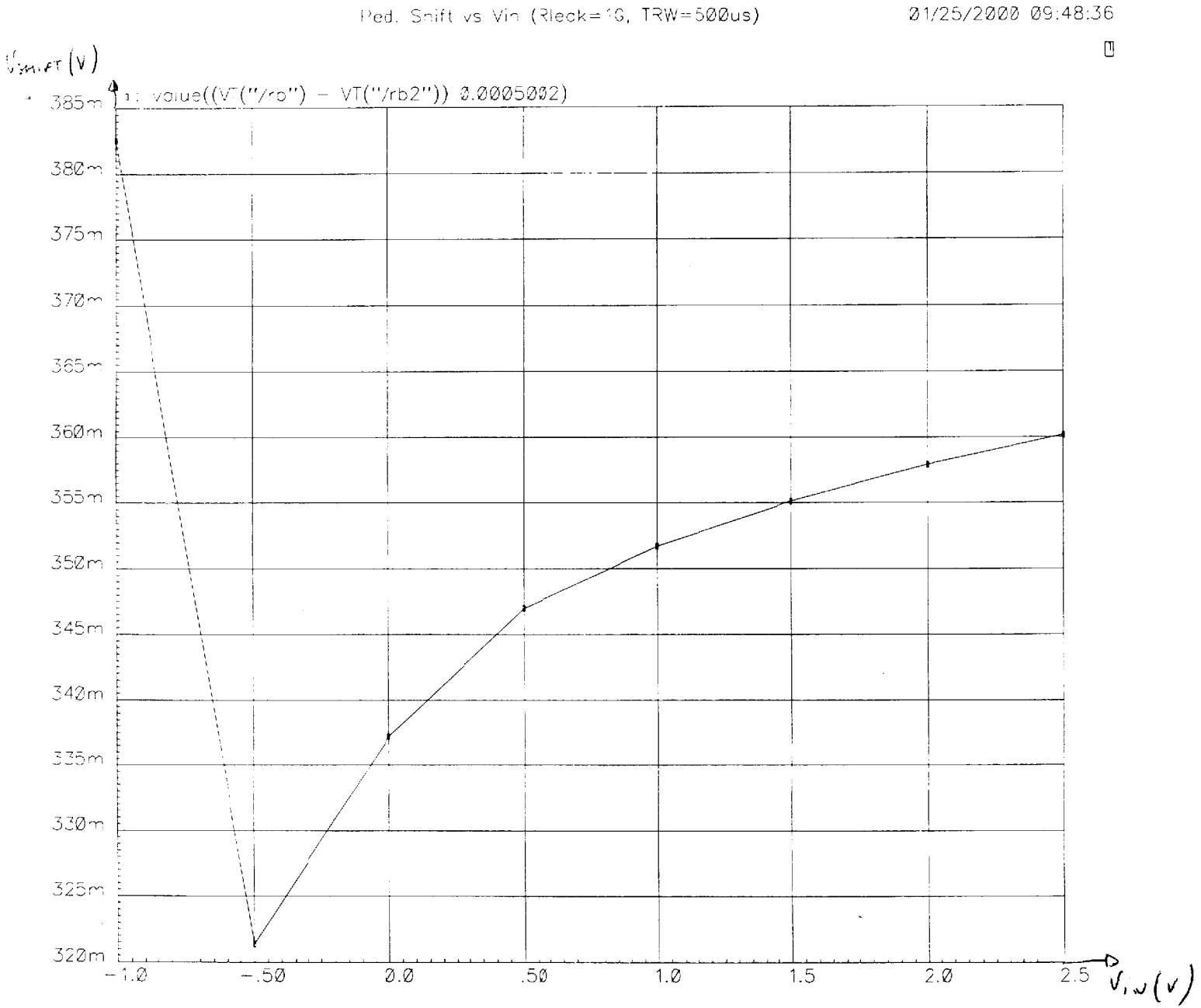


Fig 9 pedestal shift variation vs t_{RW}
$R_{leak} = 26\,\Omega$


Ped. Shift vs Vin (Rleck=1G, TRW=500us)
01/25/2000 09:48:36
1: value((VT("/rb") - VT("/rb2")) 0.0005002)
385m
380m
375m
370m
365m
360m
355m
350m
345m
340m
335m
330m
325m
320m
-1.0
-.50
0.0
.50
1.0
1.5
2.0
2.5

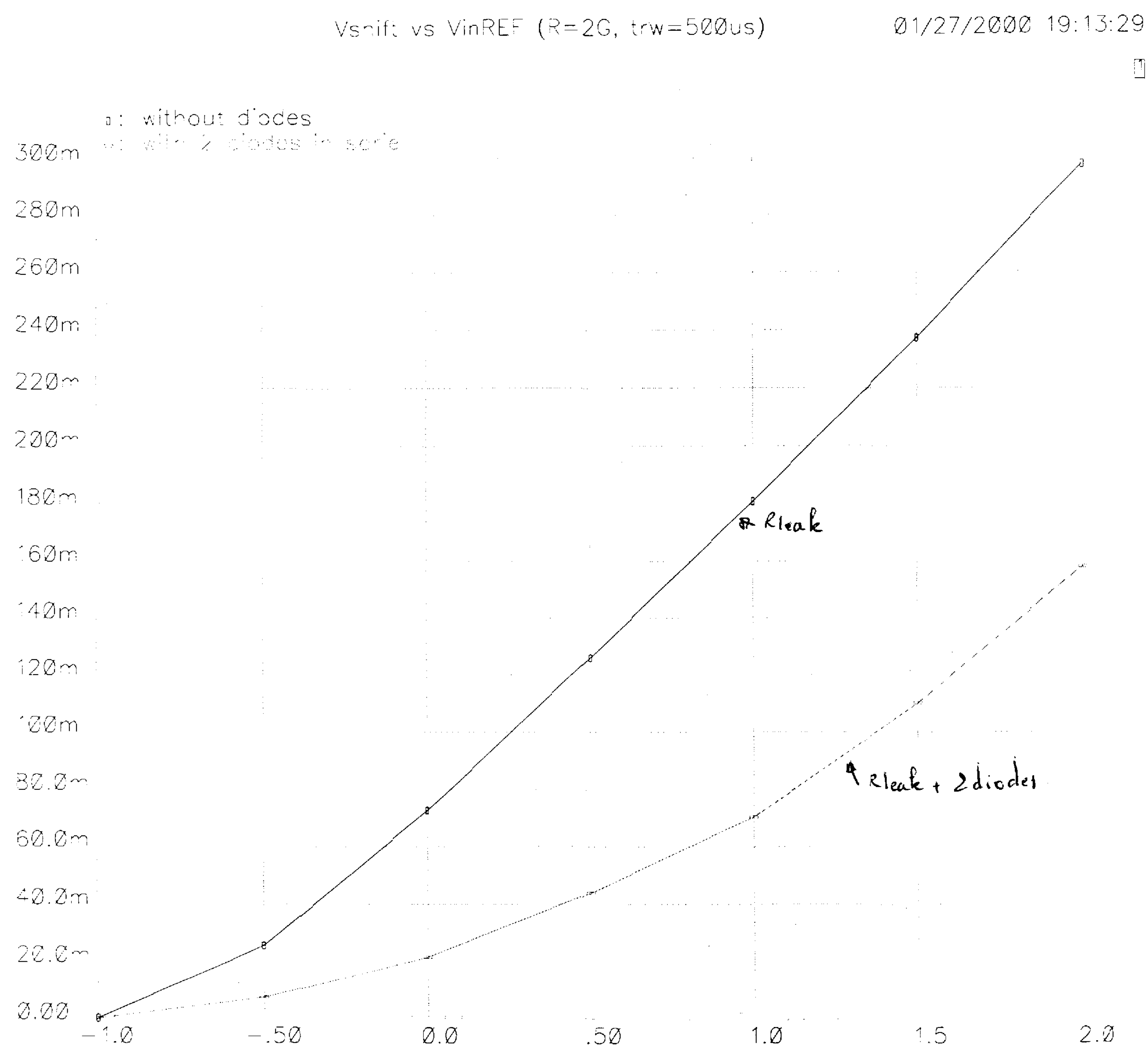


Fig 11 Simulated Pedestal Shift due to leakage vs VREFIN